Product Specification
XENPAK 10G SR 03km SC Optical Transceiver

1. Features

- XAUI Electrical Interface: 4 Lanes @ 3.125Gbit/s
- 850nm Vcsel
- Hot Z-Pluggable
- SC-Duplex Optical Receptacle
- MDIO, DOM Support
- Pin Photo-detector
- Compliant to XENPAK MSA
- Compliant to IEEE 802.3ae 10GBASE-SR Application
- Operating Case Temperature: 0°C to 70°C

2. Reference

- IEEE 802.3ae as 10GBASE-SR, XENPAK MSA Release3.0

3. Product Description

XGIGA's 10Gb/s XENPAK transceiver module XENPAK 10G SR 03km SC is a hot pluggable in the Z-direction module that is usable in typical router line card applications, Storage, IP network and LAN and compliant to XENPAK MSA. The XENPAK 10G SR 03km SC is a fully integrated 10.3Gbit/s optical transceiver module that consists of a 10.3Gbit/s optical transmitter and receiver, XAUI interface, Mux and Demux with clock and data recovery(CDR). This version of XGIGA Inc. transceiver line uses an 850nm Vcsel Laser Diode to achieve 300m over 50/125 multi-mode fiber as 10GBASE-SR of the IEEE 802.3ae.

4. Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Center Wavelength	λ_C	840	850	860	nm
Signaling speed		-	10.3125	-	Gbit/s
Signaling speed variation from nominal		-100	-	+100	ppm
Average Optical Power	Pf	-7.3	-	-1.3	dBm
Side Mode Suppression Ratio	Sr	30	-	-	dB [1]
Extinction Ratio	Er	3.5	-	-	dB
Off Transmit Power	Poff	-	-	-30	dBm [1]
Receiver Sensitivity	Rsense	-		-11.1	dBm
Receiver Overload	Rro	+0.5	-	-	dBm [1]
Optical Centre Wavelength	AC	840		860	nm
Los D-Assert	ROSd			-12	dBm
Los Assert	ROSa	-30			dBm
Los Hysteresis		0.5	-	-	dB

Notes:
[1] Average

5. Electrical Performance

5.1. Power Supply Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Supply Voltage	V_{CC1}	3.135	3.300	3.465	V
Supply Voltage	V_{CC2}	1.152	1.200	1.248	V
Supply Current	I_{CC1}	-	-	1.0	A [1]
Supply Current	I_{CC2}	-	-	1.7	A [2]
Power Consumption	P_{DS}	-	-	4.0	W
Power supply stabilization time	T_{DF}	-	-	500	ms
Initialization Time	T_{INIT}	-	-	5	s
RESET Assert Time	T_{RESET}	1	-	-	ms
Hold Time after rising edge of RESET	T_{HOLD}	500	-	-	ms

Notes:
[1] +3.3 V
[2] APS

5.2. XAUI Driver Characteristics

Parameter	Min.	Typ.	Max.	Unit
Baud Rate	-	3.125	-	Gbit/s
Baud Rate Tolerance	-100	-	+100	ppm
Differential Amplitude	800	-	1600	mVPP [1]

Notes:
[1] AC, near-end value

5.3. 1.2V CMOS Interface Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Input High Voltage	V_{IH}	0.84	-	1.5	V
Input Low Voltage	V_{IL}	-0.3	-	0.36	V
Input Pull-down Current	I_{In}	20	40	120	µA [2]
Output High Voltage	V_{OH}	1.0	-	-	V [3]
Output Low Voltage	V_{OL}	-	-	0.2	V [3]
Pull up Resistance	R_{LASI}	10	-	22	k ohm
Capacitance	C_{LASI}	-	-	10	pF
Load Capacitance	C_{Load}	-	-	320	pF

Notes:
[1] AC
[2] Vih=1.2V
[3] Pull-up=10k ohm to 1.2 V

5.4. MDIO Bidirectional Interface Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units
Input High Voltage	V_{IHM}	0.84	-	1.5	V
Input Low Voltage	V_{ILM}	-0.3	-	0.36	V
Output High Voltage	V_{OHM}	1.0	-	1.5	V
Output Low Voltage	V_{OLM}	-0.3	-	0.2	V
Pull up Resistance	R_{MDIO}	200	-		Ohm
MDC min high/low time	T_{HM}, T_{LM}	160	-	-	ns
MDC Frequency	$1/T_{CK}$	T_{BD}	-	2.5	MHz
Setup time	T_{DIS}	10	-	-	ns
Hold time	T_{DIH}	10	-	-	ns
MDIO output delay after rising edge of MDC	T_{PD}	0	-	300	ns
Input Capacitance	Ci	-	-	10	pF
Bus Loading	C_L	-	-	470	pF

Notes:

The maximum value of R_{MDIO} depends on bus loading (C_L) , input capacitance (Ci), and MDC frequency ($1/T_{CK}$).

6. XENPAK Pin Configuration

Pin	Symbol	I/O	Logic	Description
1	GND	I	Supply	Electrical ground
2	GND	I	Supply	Electrical ground
3	GND	I	Supply	Electrical ground
4	RESERVED	-	-	Reserved
5	3.3 V	I	Supply	Power
6	3.3 V	I	Supply	Power
7	APS	I	Supply	Adaptive Power Supply
8	APS	I	Supply	Adaptive Power Supply
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.
10	RESET	I	1.2 V CMOS	TX OFF when MDIO RESET
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.
12	TX ON/OFF	I	1.2 V CMOS	Transmitter ON/OFF
13	RESERVED	-	-	Reserved
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.
17	MDIO	I/0	Open Drain	Management Data IO
18	MDC	I	1.2 V CMOS	Management Data Clock
19	PRTAD4	I	1.2 V CMOS	Port Address bit 4 (Low=0)
20	PRTAD3	I	1.2 V CMOS	Port Address bit 3 (Low=0)
21	PRTAD2	I	1.2 V CMOS	Port Address bit 2 (Low=0)
22	PRTAD1	I	1.2 V CMOS	Port Address bit 1 (Low=0)
23	PRTAD0	I	1.2 V CMOS	Port Address bit 0 (Low=0)
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.
25	APS SET	O	-	Feedback output for APS
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.
27	APS SENSE	O	Analog	APS Sense Connection
28	APS	I	Supply	Adaptive Power Supply
29	APS	I	Supply	Adaptive Power Supply
30	3.3 V	I	Supply	Power
31	3.3 V	I	Supply	Power

Pin	Symbol	I/O	Logic	Description
32	RESERVED	-	-	Reserved
33	GND	I	Supply	Electrical Ground
34	GND	I	Supply	Electrical Ground
35	GND	I	Supply	Electrical Ground
36	GND	I	Supply	Electrical Ground
37	GND	I	Supply	Electrical Ground
38	RESERVED	-	-	Reserved
39	RESERVED	-	-	Reserved
40	GND	I	Supply	Electrical Ground
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-
43	GND	I	Supply	Electrical Ground
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-
46	GND	I	Supply	Electrical Ground
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-
49	GND	I	Supply	Electrical Ground
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-
52	GND	I	Supply	Electrical Ground
53	GND	I	Supply	Electrical Ground
54	GND	I	Supply	Electrical Ground
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-
57	GND	I	Supply	Electrical Ground
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-
60	GND	I	Supply	Electrical Ground
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-
63	GND	I	Supply	Electrical Ground
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-
66	GND	I	Supply	Electrical Ground
67	RESERVED	-	-	Reserved

Pin	Symbol	I/O	Logic	Description
68	RESERVED	-	-	Reserved
69	GND	I	Supply	Electrical Ground
70	GND	I	Supply	Electrical Ground

Notes:

Case is connected to electrical ground in the module.

7. Mechanical dimensions

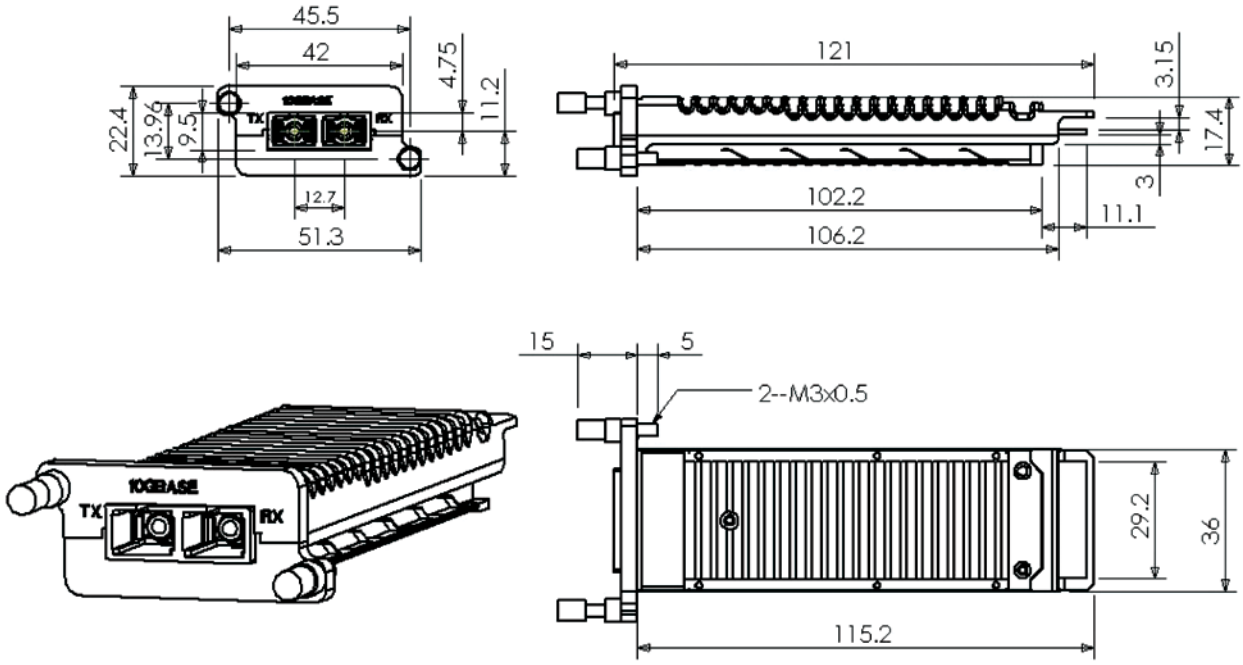

Figure 2. Mechanical dimensions.

8. Register Definition

Device Address (Dec) Register Address (Hex)	PMA/PMD 1	PCS 3	PHY XS 4
0x0000	PMA/PMD Control1	PCS Control1	PHY XS Control1
0x0001	PMA/PMD Status1	PCS Status1	PHY XS Status1
0x0002	PMA/PMD Device Identifier0	PCS Device Identifier0	PHY XS Device Identifier0
0x0003	PMA/PMD Device Identifier1	PCS Device Identifier1	PHY XS Device Identifier1

Device Address (Dec) Register Address (Hex)	PMA/PMD 1	PCS 3	PHY XS 4
0x0004	PMA/PMD Speed Ability	PCS Speed Ability	PHY XS Speed Ability
0x0005	PMA/PMD Device in Package1	PCS Device in Package1	PHY XS Device in Package1
0x0006	PMA/PMD Device in Package2	PCS Device in Package2	PHY XS Device in Package2
0x0007	10G PMA/PMD Control2	PCS Control2	Reserved
0x0008	10G PMA/PMD Status2	PCS Status2	PHY XS Status2
0x0009	10G PMD Transmit Disable	Reserved	Reserved
0x000A	10G PMD Receive Signal O.K.	Reserved	Reserved
0x000E	Package Identifier0	Reserved	Reserved
0x000F	Package Identifier1	Reserved	Reserved
0x0018	Reserved	Reserved	10G PHY XGXS Lane Status
0x0019	Reserved	Reserved	10G PHY XGXS Test Control
0x0020	Reserved	10GBASE-R PCS Status1	Reserved
0x0021	Reserved	10GBASE-R PCS Status2	Reserved
0x0022	Reserved	10GBASE-R PCS Test pattern Seed A0	Reserved
0x0023	Reserved	10GBASE-R PCS Test pattern Seed A1	Reserved
0x0024	Reserved	10GBASE-R PCS Test pattern Seed A2	Reserved
0x0025	Reserved	10GBASE-R PCS Test pattern Seed A3	Reserved
0x0026	Reserved	10GBASE-R PCS Test pattern Seed B0	Reserved
0x0027	Reserved	10GBASE-R PCS Test pattern Seed B1	Reserved
0x0028	Reserved	10GBASE-R PCS Test pattern Seed B2	Reserved
0x0029	Reserved	10GBASE-R PCS Test pattern Seed B3	Reserved
0x002A	Reserved	10GBASE-R PCS Test pattern Control	Reserved
0x002B	Reserved	10GBASE-R PCS Test pattern Error counter	Reserved
0x8000	NVR Control/Status (XENPAK Register)	Reserved	Reserved
0x8007 - 0x807D	NVR (XENPAK Register)	Reserved	
0x807E- 0x80AD	Customer AREA	Reserved	
0x80AE - 0x8106	XGIGA Specific Area(XENPAK Register)	Reserved	
0x9000	RX_ALARM Control (XENPAK Register)	Reserved	
0x9001	TX_ALARM Control (XENPAK Register)	Reserved	

Device Address (Dec) Register Address (Hex)	PMA/PMD 1	PCS 3	PHY XS 4
0x9002	LASI Control (XENPAK Register)	Reserved	
0x9003	RX_ALARM Status (XENPAK Register)	Reserved	
0x9004	TX_ALARM Status (XENPAK Register)	Reserved	
0x9005	LASI Status (XENPAK Register)	Reserved	
0x9006	TX_FLAG Control Bits	Reserved	
0x9007	RX_FLAG Control Bits	Reserved	
0xA000 - 0xA027	Alarm and Warning Thresholds	Reserved	
0xA060 - 0xA069	Digital Optical Monitoring Interface	Reserved	
0xA06F	DOM Capability - Extended	Reserved	
0xA070	TX_ALARM_FLAG Bits	Reserved	
0xA071	RX_ALARM_FLAG Bits	Reserved	
0xA074	TX_WARNING_FLAG Bits	Reserved	
0xA075	RX_WARNING_FLAG Bits	Reserved	
0xA100	Optional Digital Optical Monitoring (DOM) Control/ Status	Reserved	